

Atomic Layer Deposition: Enabling Advanced High-k and Metal Films

Introduction

Atomic layer deposition (ALD) has emerged as an enabling technology for microelectronic device fabrication and is actively being investigated for application in emerging technology areas. ALD was first invented in 1977 by Dr. Tuomo Suntola to deposit zinc sulfide films from ZnCl_2 and H_2S for use in electroluminescent devices. While this technique has been utilized for a number of years for a variety of applications ranging from LCD panel manufacturing to industrial coatings, it is now being exploited in the production of advanced microelectronics for high-k dielectric and metal films in transistor gate stacks and capacitors, Cu barrier/seed films, etch-stop layers and a variety of gap layers and diffusion barriers for thin-film, magnetic head and non-volatile memory applications.

The ALD process has intrinsic advantages over traditional deposition processes such as (metal organic) chemical vapor deposition ((MO)CVD) and physical vapor deposition (PVD). Capitalizing on surface saturation reactions, ALD processes have inherent thickness control and are highly stable, being insensitive to fluctuations in both temperature and reactant flux. The resulting films are pure, dense, smooth and highly conformal, attaining perfect step-coverage on feature aspect ratios as high as 100:1. With an optimized ALD process, excellent film-adhesion, composition control, uniformity and repeatability have been observed. Since ALD films are formed layer-by-layer, both laminate structures with abrupt transitions or mixed films with graded elemental profiles can be readily achieved. ALD processes also keep with the industry trend to move to lower thermal budget processing as most processes perform well below 400 °C while conventional CVD processes typically operate at temperatures above 500 °C.

Fundamentals of Atomic Layer Deposition

The basic steps of ALD processing are illustrated in Figure 1. The deposition process is conducted on a substrate functionalized with reactive surface moieties. The first precursor is introduced into the reactor and allowed to chemisorb on the substrate until the surface is saturated. The excess precursor is then evacuated/purged from the system. The second precursor is then delivered to the reactor and allowed to react with the adsorbed species on the substrate. Excess precursor and reaction byproducts are again removed from the system by pumping and/or inert gas purge. The result is a surface saturated with up to a monolayer of the desired compound. Sequential repetition of the ALD cycle results in layer-by-layer growth with precise control of the deposition thickness.

Since ALD is based on self-limiting growth during alternating reactions, the process must be fine-tuned for optimum results. Even though the unique surface reaction characteristics for ALD have reduced the strict requirements for temperature, pressure, and concentration of CVD processes, ALD parameters must still be optimized to realize such benefits as accurate thickness control and superior conformality. Reactor temperature is one of the most important parameters used to control surface saturation. As the very foundation of the ALD process, reactor temperature plays two major roles: it provides the activation energy for ALD reaction and it helps to desorb the excess reactants and by-products following monolayer formation. Figure 2 defines the optimal ALD process temperature window for monolayer coverage. The ALD window is related to precursor choice, dose, and purging. To achieve full monolayer coverage, a sufficient dose of a thermodynamically stable precursor—one that does not decompose at reactor temperature—is delivered to the substrate. Overdosing is often used to achieve full surface saturation. Several parameters can be used to control the doses of the precursors: source temperature, source flows, partial pressures of the precursors, and the total reactor pressure.

The saturation curve in Figure 3 illustrates the self limiting nature of the ALD process. The growth rate increases linearly with pulse time until saturation conditions are achieved. When saturation is achieved, the growth rate is constant and doesn't change with increasing pulse time. However, growth rates can increase significantly if there is a parasitic CVD growth component or precursor decomposition. Hence, saturation curves are typically used to determine the purity of the ALD process. Growth rates of ALD processes range from 0.3 Å to 1.5 Å per ALD cycle. Although these growth rates can be tolerated for very thin film applications (< 200 Å), cycle time is of paramount importance when ALD is to be used for thicker films.

As ALD is being evaluated and adopted in many areas of semiconductor manufacturing, selection of the appropriate precursor becomes extremely important. There are several 'ideal' properties that an ALD precursor should exhibit. The precursor should be sufficiently volatile, should have a reproducible vaporization rate, ideally should not self-react or decompose at the deposition temperature, should be highly reactive to the complementary precursor, should create volatile reaction byproducts and for growth rate and nucleation reasons, should have optimal ligand sizes. The general trend in precursor selection is moving to the liquid organometallics due to their ease of use – but film properties and application specific targets (for example, impurity levels, electrical performance, etc) overwhelmingly dictate chemical selection. Furthermore, cost of ownership concerns dictate that the precursors be cost competitive with competing, conventional deposition processes. ALD has a very high precursor utilization efficiency that often offsets the high cost of novel precursors. Typical precursor types used in ALD are illustrated in Figure 4. As ALD moves into volume manufacturing, and the industry narrows to a select few precursors, the cost concerns will likely be mitigated as chemical suppliers streamline their production processes. With currently available precursors, a wide variety of ALD films can be deposited (Figure 5).

Variations of Atomic Layer Deposition

Although ALD was first conceived as a purely thermal process, slight variations on the basic ALD cycle have been devised over the years. The most common variation is the plasma enhanced atomic layer deposition process (PEALD). PEALD can eliminate one of the steps of the ALD cycle, enabling a further reduction of cycle times. With the PEALD process, complementary precursors that do not react with each other at the deposition temperature are introduced to the reactor at the same time. The source precursor is then shut off and allowed to purge from the reactor. This is followed by a pulse of direct plasma. The plasma environment creates highly reactive radicals that can react with the source precursor adsorbed on the substrate. Shutting off the plasma quickly removes the source of the reactive radicals, and the constant flow in the reactor purges the volume of any excess radicals and reaction by-products (Figure 6). In addition to higher growth rates and shorter cycle times, PEALD films can exhibit higher densities and higher breakdown voltages than conventional thermal ALD films. The technique has gained traction in multiple applications such as DRAM, MIM and eDRAM dielectric films. However, in critical thin film applications such as high power gate dielectrics, concerns of plasma damage and interface oxidation has kept the technique from being widely adopted. A second concern is the ability for radicals to diffuse to the bottom of tight opening/high aspect ratios, which can reduce conformality. PEALD also is being actively investigated for the deposition of metal ALD films as these films typically suffer from very low growth rates with conventional thermal processes.

Hardware Designs

ALD equipment designs can be divided into two general categories: hot wall and cold wall reactors. Hot wall reactors maintain the entire reactor at or near the deposition temperature. The primary advantage of hot wall reactors is that all the deposition on the reactor walls is a quality ALD film. Hot wall reactors tend to resist premature film delamination and allow quick purging of the reaction space due the higher precursor desorption flux from the heated walls. Cold wall reactors usually only have the substrate heated to the deposition temperature while other reactor components are kept at a lower temperature. This allows delivery of precursors that may decompose at the deposition temperatures, but risk being susceptible to longer purge times, and therefore, a greater CVD component due to the reduced rate of desorption of precursors from the cold wall surfaces. These effects can worsen as film deposition accumulates in the chamber.

Different configurations of ALD equipment are available for semiconductor manufacturing. ALD reactors can be single wafer tools, mini-batch (< 25 wafer loads) tools, or large batch (50 – 100 wafer loads) systems. Single wafer tools allow ultimate process control while batch systems offer substantial gains in productivity. Selection of the appropriate tool set is driven by film requirements for the application. Furthermore, some ALD films are very difficult to deposit uniformly in batch systems necessitating the use of single wafer or mini-batch equipment. ASM International, N.V, offers multiple ALD solutions: the Pulsar[®] 3000 thermal ALD module, the EmerALD[™] 3000 PEALD

module, the A412TM batch ALD system, and the StellarTM 3000 PEALD system. These offerings cover the entire breadth of semiconductor ALD application needs.

Figure 7 shows a schematic layout of a hot-wall, cross-flow ALD reactor. In this reactor, the reactant and purge gases are introduced at the front of the reactor via a gas distributor. The gas stream, which is characterized by a laminar plug-flow profile, moves across the surface of the wafer and exits the back of the reactor to a vacuum pump. This reactor type is used in the ASM Pulsar[®] 3000 module. Reactor volume and flow cross-sections are minimized for optimum purging efficiency. A schematic layout of a typical showerhead reactor is shown in Figure 8. Here the reactant and purge gas is introduced above the wafer, with gas flow directed downward and radially outward from the center to the edge of the wafer. This reactor type is used in the ASM EmerALDTM 3000 module. This reactor is also equipped with a direct plasma generator to enable PEALD processing.

Applications

Since the invention of the MOS transistor, SiO₂, and later on SiON have been the perfect gate dielectric materials, allowing scaling from a thickness of 1000 Å to approximately 10 Å. This has enabled the number of transistors placed in integrated circuits to double approximately every 24 months (Moore's law) [1], and to shrink transistor geometries in production devices to the 65 nm technology node. Further scaling of the SiO₂ gate thickness causes excessive power dissipation due to gate leakage from quantum mechanical tunneling of electrons through the extremely thin gate oxide. Thicker high-k dielectrics are replacements of SiO₂ or SiON gate dielectrics to reduce leakage currents. Gate dielectric thicknesses are expressed as equivalent oxide thickness (EOT) where:

$$EOT = (k_{SiO_2}/k_{HK})/t_{ox}$$

k_{SiO_2} is the dielectric constant of SiO₂, k_{HK} is the dielectric constant of the high-k dielectric material, and t_{ox} is the physical thickness of the high-k film. Using high-k materials allow deposition of thicker films while maintaining the scaling of EOT [2-4]. Gate oxide high-k materials must be deposited, replacing the thermal oxidation processes that have been used for decades in the critical gate oxide process. This is an astronomical change in the semiconductor industry as a deposition process must now achieve the uniformities and defect performance of oxidation furnaces. ALD is a natural choice due to its ability to deposit highly uniform and dense films, with extremely tight thickness control, and low defectivity. Leaders in the industry are introducing high-k gate dielectrics with Hf-based compounds at the 45 nm technology node. Others are expected to implement a high-k gate solution by the 32 nm node.

When the SiO₂ gate is replaced with a high-k material, the traditional polysilicon gate must be replaced by a metal gate to realize the full electrical benefit. Polysilicon gate electrodes have been found to be incompatible with high-k dielectrics due to Fermi level pinning effects, poly depletion and chemical instability [5]. Figure 9 shows a comparison of the gate leakage currents achievable with SiO₂ and HfO₂ gate dielectrics. At the same

EOT values, the HfO₂/TiN gate stack shows reduction in leakage current by many orders of magnitude when compared with the traditional SiO₂/Poly-Si gate stack. However, integration of metal gates into the gate process module is extremely complex. The appropriate choice of metal is critical as electrode work functions must be tuned appropriately for proper operation of the CMOS device. This may ultimately result in the use of a dual metal gate solution – one for the NMOS transistor and the other for the PMOS transistor. Post processing of the device can also affect the work function of the metal electrode, resulting in a shift in electrical performance. High temperature processing (~ 1000 C), like source/drain dopant activation anneals, can shift the work function of the metal electrode and cause crystallization of the high-k dielectric. Several techniques to mitigate these effects have been investigated, including using thin cap layers between the gate dielectric and the metal gate to assist in work function tuning [6], and addition of ZrO₂ to HfO₂ films to stabilize the high-k dielectric during high temperature processing [7]. Figures 10 and 11 highlight the benefits of these techniques. Gate last process flows can also avoid exposing the gate dielectric to high temperature processing by depositing the gate films after the activation anneals, inside an area defined by gate spacers. Perfect step coverage is required which makes ALD the perfect choice in processing technique.

While pure high-k gate dielectrics are being pursued for high performance devices such as desktop and server processors, hafnium silicate is becoming the material of choice for low standby power devices. Silicate films provide a good balance between performance and leakage, enabling improved battery life in low power mobile applications such as notebook computers and mobile phones. ALD of hafnium silicate allows precise stoichiometric control of the films. Figure 12 shows gate leakage current as a function of EOT for HfSiO layers with different compositions and thicknesses. The gate leakage mainly depends on the physical thickness of the layer, with the k-value of the film increasing with increasing Hf percentage in the film. It has been shown that Hf-rich silicates meet all specifications for the 45 nm LSTP node with room for further scaling [8].

The first volume adoption of ALD in semiconductor manufacturing was in DRAM technology. DRAM design has been aggressively scaling cell sizes in order to increase capacitance density and reduce the cost per bit of memory. ALD is a natural choice due its ability to deposit high quality layers in the very high aspect ratio trench structures used in DRAM design and high k dielectrics deposited by ALD allow further scaling of EOTs. ALD Al₂O₃ has been employed in DRAM manufacturing since early 2000, and more recently, laminate structures such as Al₂O₃/HfO₂ and Al₂O₃/ZrO₂ stacks have been gaining traction. PEALD has also been demonstrated in eDRAM manufacturing [9]. The capacitors meet all specifications for EOT (<8 Å), leakage current (<1 fA/cell at 125 C) and lifetime (>10 years at V_{dd}=1V). Figure 13 shows the typical conformality of ALD films in the deep trench structures and hemispherical grain silicon structures used in DRAM production. Metal ALD films such as TiN are also widely being used as capacitor electrodes in DRAM manufacturing.

ALD is also being widely investigated for the deposition of dielectrics and metals for non-volatile memory applications. Flash technology has been dominated by floating gate technology (Figure 14). High-k dielectrics are being investigated as a replacement for SiO_2 and Si_3N_4 as the inter-poly dielectric in order to improve the capacitance coupling ratio between the floating gate and control gate. As cell sizes shrink, aspect ratios for the deposition of the inter-poly dielectric increase, necessitating the need for a conformal coating technique such as ALD. By 2010, floating gate technology is expected to be replaced by alternatives such as charge trapping memories (TANOS, NROM), phase change memory (PCM), and ferroelectric memory (FeRAM). 3-D stackable memory is also being investigated. ALD is already being used as blocking layers and diffusion barriers for these technologies.

ALD films are also emerging in the fabrication of passive components integrated directly within the chip at the interconnect level. Examples include RF capacitors for oscillators, phase shift network, analog capacitors for A/D and D/A converters and decoupling capacitors. These capacitors must have low leakage currents, high dielectric breakdown voltage, and high stability over a broad voltage range. ALD Al_2O_3 , HfO_2 , Ta_2O_5 and stacks of these films have been investigated for these applications. PEALD Ta_2O_5 films have been demonstrated as an improved alternative to MOCVD films for decoupling capacitor applications due to improved density and impurity levels [10].

Outside of the semiconductor industry, ALD is emerging as a key enabling technology. ALD Al_2O_3 has been used for a number of years in the fabrication of thin film magnetic heads (TFMH). TFMHs are complex structures consisting of multiple thin metal and dielectric films. ALD layers are being used as gap dielectric layers within the head structure and as encapsulating layers when wafer level processing is completed. The gap dielectric layers separate the conductive shield and pole layers in the TFMH, serving to channel the magnetic fields from the disk into the read sensor. These layers also isolate the read sensor magnetically from the write head. To achieve higher areal density, the TFMH structure must be scaled, requiring a reduction in the gap dielectric thickness. Scaling increases the substrate topography to aspect ratios above 10:1. PVD and ion beam deposition (IBD) techniques suffer from conformality and reliability issues [11], resulting in ALD being the clear deposition technique of choice. The ability to deposit extremely pure, dense and conformal layers with ALD provides a substantial advantage for a wide range of functions such as wear layers, diffusion barriers and encapsulation films.

Conclusions

ALD is an enabling process technology with far reaching applications in the semiconductor industry. Device scaling has resulted in the thinning of dielectric films past their physical and electrical limits and higher aspect ratios are now commonplace in device architecture. As conventional deposition techniques are challenged to meet the extremely critical demands for film quality and conformality in progressive technologies,

ALD has demonstrated the ability to meet these demands with additional room for further scaling.

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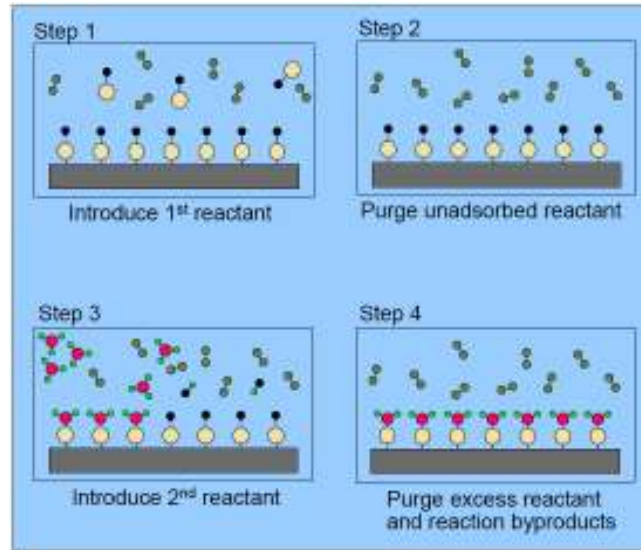


Figure 1. Schematic of ALD Growth mechanism

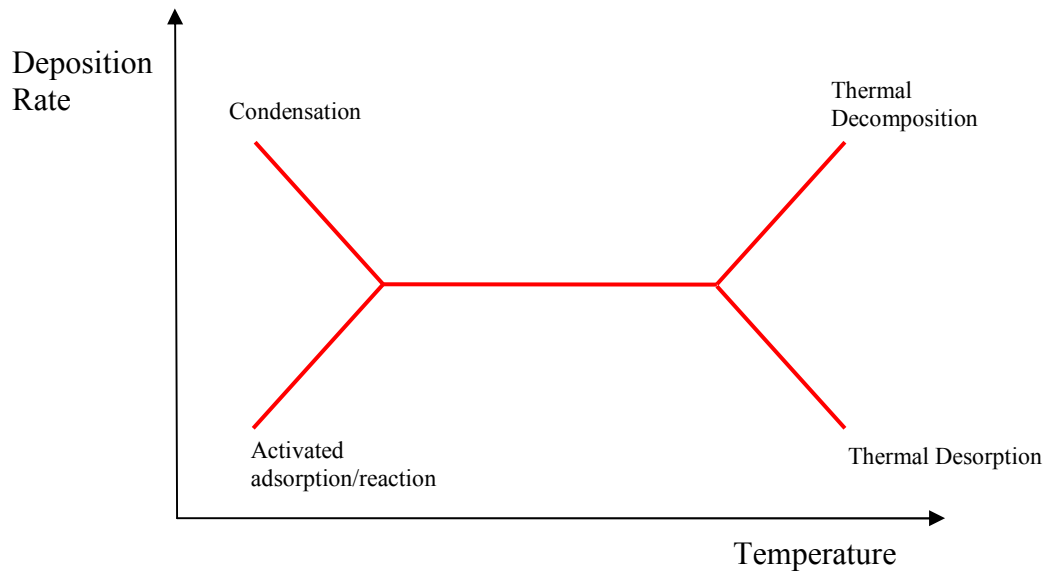


Figure 2. The ALD Process Window

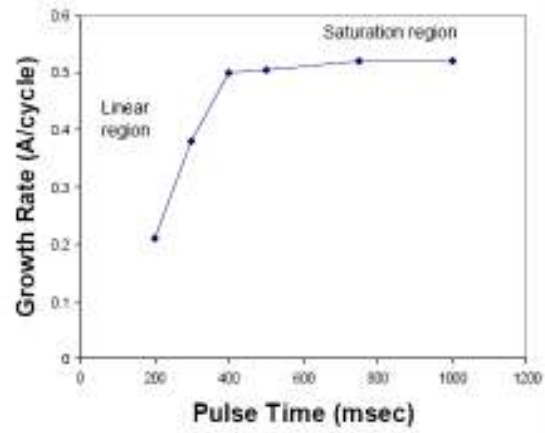


Figure 3. ALD Saturation Curve

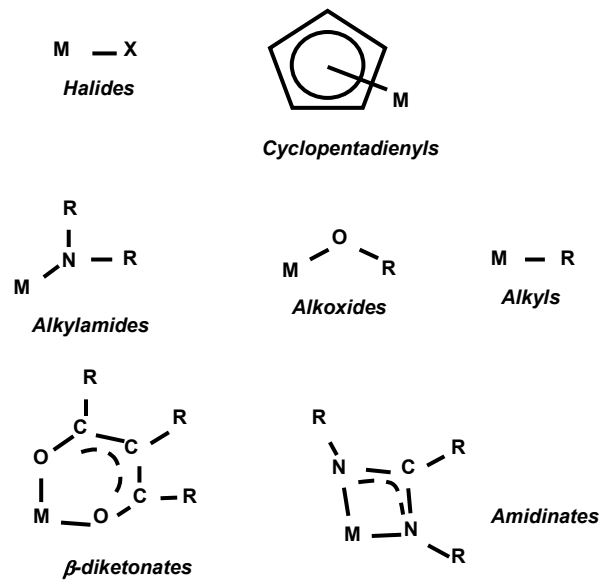


Figure 4. Typical ALD precursors

II-VI compounds	ZnS, ZnSe, ZnTe, ZnS _{1-x} Se _x CaS, SrS, BaS, SrS _{1-x} Se _x CdS, CdTe, MnTe, HgTe, Hg _{1-x} Cd _x Te, Cd _{1-x} Mn _x Te
II-VI based TFEL phosphors	ZnS:M (M = Mn, Tb, Tm), CaS:M (M = Eu, Ce, Tb, Pb), SrS:M (M = Ce, Tb, Pb)
III-V compounds	GaAs, AlAs, AlP, InP, GaP, InAs Al _x Ga _{1-x} As, Ga _x In _{1-x} As, Ga _x In _{1-x} P
Nitrides	
Semiconductors/Dielectric	AlN, GaN, InN, SiN _x , Ta ₃ N ₅
Metallic	TiN, Ti-Si-N, TaN, NbN, MoN, W ₂ N, WNC
Oxides	
Dielectric	Al ₂ O ₃ , TiO ₂ , ZrO ₂ , HfO ₂ , Ta ₂ O ₅ , Nb ₂ O ₅ , Y ₂ O ₃ , MgO, CeO ₂ , SiO ₂ , La ₂ O ₃ , SrTiO ₃ , BaTiO ₃ , Bi _x Ti _y O _z
Transparent conductors/ Semiconductors	In ₂ O ₃ , In ₂ O ₃ :Sn, In ₂ O ₃ :F, In ₂ O ₃ :Zr, SnO ₂ , SnO ₂ :Sb, ZnO, ZnO:Al, ZnO:B, ZnO:Ga, Ga ₂ O ₃ , WO ₃ , NiO, CoO _x , MnO _x
Superconductors	YBa ₂ Cu ₃ O _{7-x}
Other ternaries	LaCoO ₃ , LaNiO ₃ , LaMnO ₃
Fluorides	CaF ₂ , SrF ₂ , ZnF ₂
Elements	Si, Ge, Cu, Ni, Mo, Ta, W, Ru, Pt, Ir, Rh, Pd
Others	La ₂ S ₃ , PbS, In ₂ S ₃ , Cu _x S, CuGaS ₂ , SiC

Figure 5. Materials Deposited by ALD
(Source: Haukka et. al. Semicon Europa 2006)

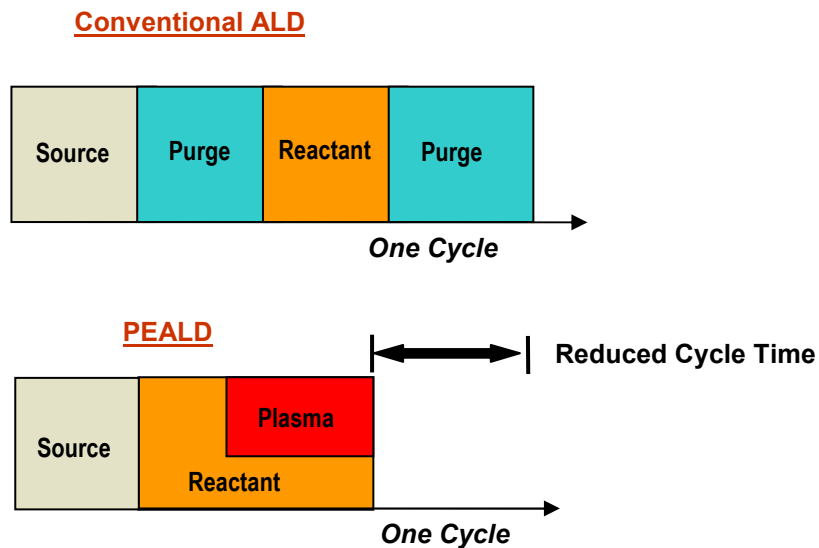


Figure 6. Thermal ALD vs. PEALD

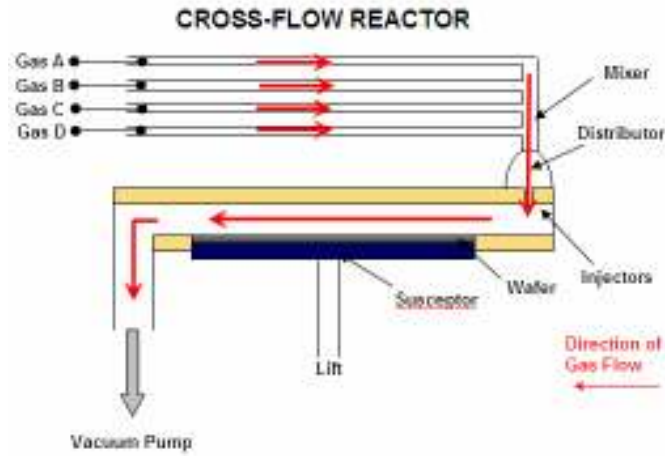


Figure 7. Cross Flow Reactor Schematic

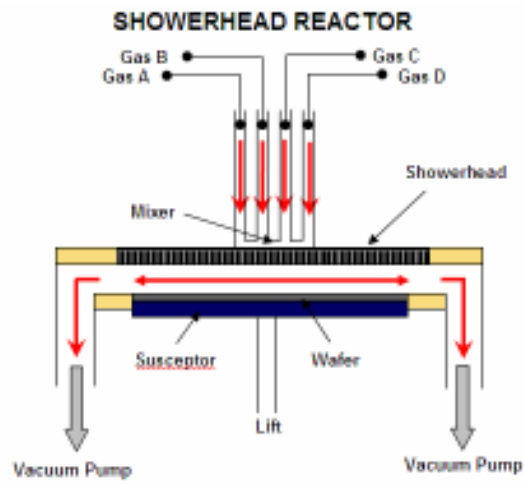


Figure 8. Showerhead Reactor Schematic

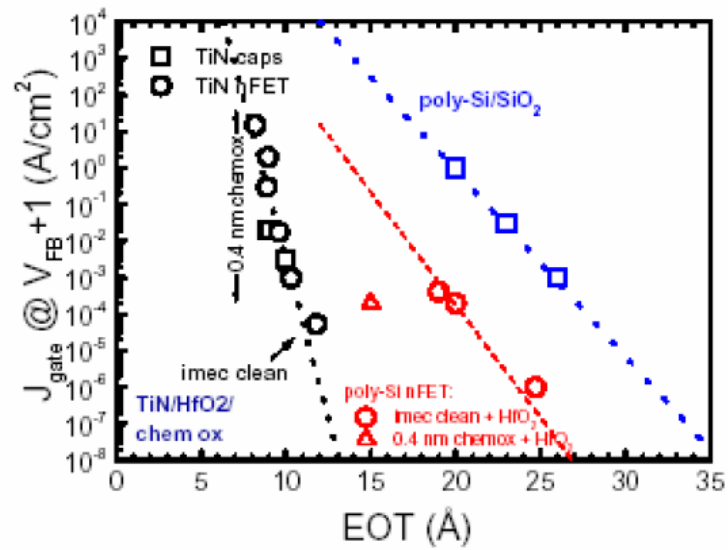


Figure 9. Scaling Advantages of High-k Dielectrics
(Source: W. Tsai et. al. IEDM 2003)

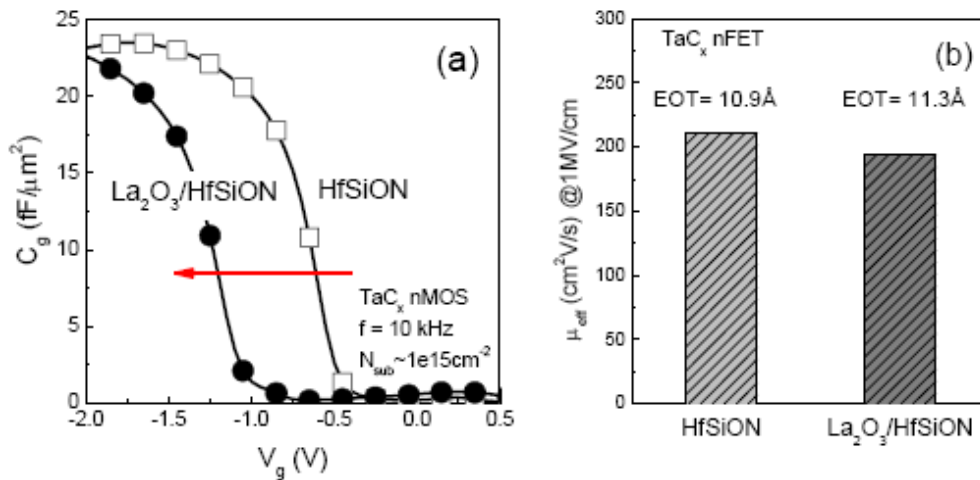


Figure 10. Workfunction Tuning Using La_2O_3 Capping Layers
(Source: H.J Cho et.al. Proceedings ICICDT 2007)

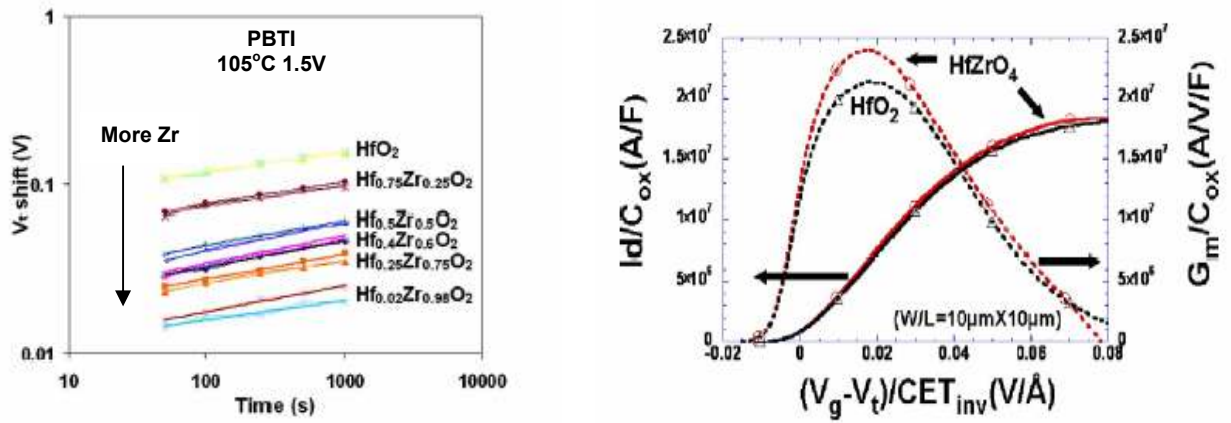


Figure 11. Reliability and Mobility Improvements by Zr Addition
(Source: Hegde et. al. SSDM 2006)

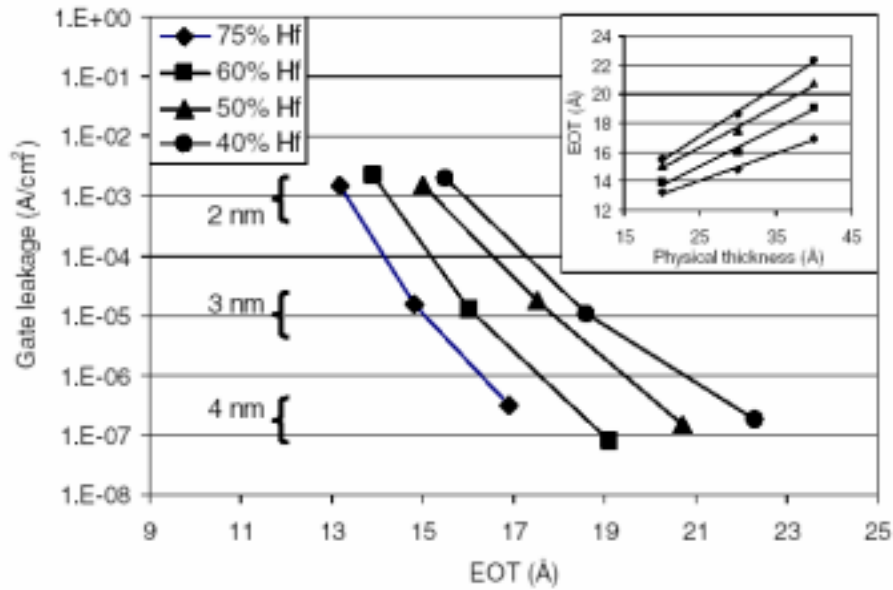


Figure 12. Hafnium Silicate Scaling by Composition Control
(Source: J. Swerts et. al., MRS Symp. Proc **917** 2006)

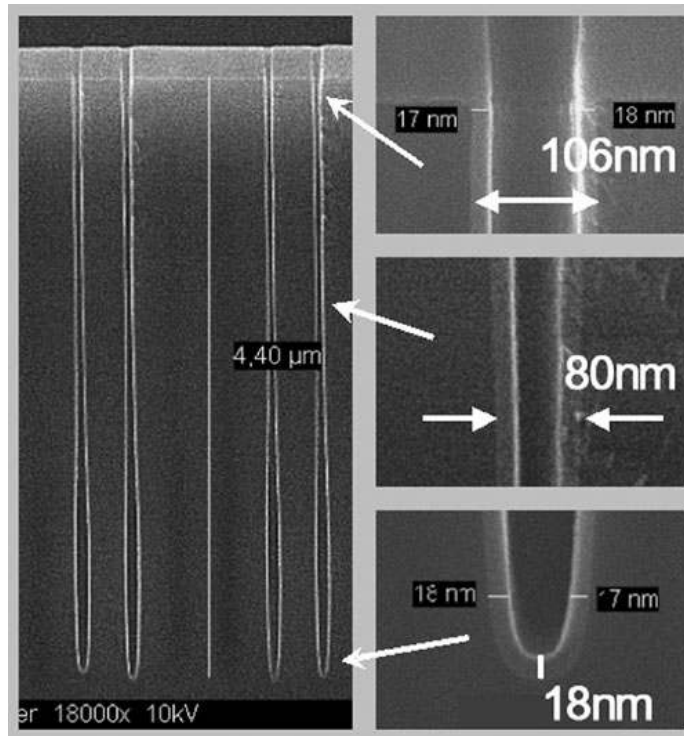


Figure 13. Conformity of ALD in Deep Trench Structures
 (Source: M. Gutsche et. al., Future Fab, 14, 2003)

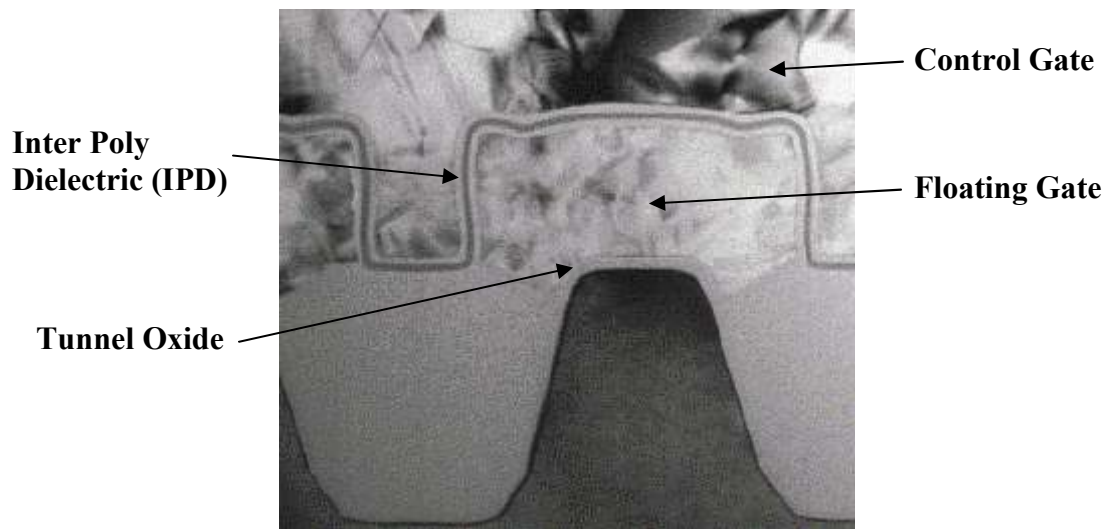


Figure 14. Floating Gate Structure for Flash Non-Volatile Memory
 (Source: A. Bergemont, EDS 2007)